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PATENT & TRADEMARK OFFICE

TSMC-02-0015C

December 17, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/679,768 10/06/03

Tuo-Hung Hou et al.

A NOVEL DUAL GATE DIELECTRIC SCHEME: SiON FOR HIGH PERFORMANCE DEVICE AND HIGH K FOR LOW POWER DEVICES

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 12/19/03

The article "Outlook on New Transistor Materials," by L. Peters in Semiconductor International, Oct. 1, 2001 edition, the next generation 70 nm and 50 nm technology nodes will need new gate dielectric materials in order to accommodate a shrinking gate size.

U.S. Patent 6,265,325 to Cao et al., "Method for Fabricating Dual Gate Dielectric Layers," describes a method for forming dual gate oxide layers having different thicknesses.

The following two U.S. Patents introduce a high k dielectric apporach for manufacturing an N-channel MOSFET and a P-channel MOSFET on the same substrate:

1) U.S. Patent 6,159,782 to Xiang et al., "Fabrication of Field Effect Transistors Having Dual Gates with Gate Dielectrics of High Dielectric Constant."

2) U.S. Patent 6,248,675 to Xiang et al., "Fabrication of Field Effect Transistors Having Dual Gates with Gate Dielectrics of High Dielectric Constant Using Lowered Temperatures."

U.S. Patent 5,960,289 to Tsui et al., "Method for Making a Dual-Thickness Gate Oxide Layer Using a Nitride/Oxide Composite Region," provides a method for fabricating a dual oxide gate structure.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

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Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-0015C	10/679,768
Applicant: Tuo-Hung Hou et al.	
Filing Date: 10/06/03	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5960289	9/28/99	Tsui et al.	438	275	6/22/98
	6159782	12/12/00	Xiang et al.	438	197	8/5/99
	6265325	7/24/01	Cao et al.	438	763	4/26/99
	6248675	6/19/01	Xiang et al.	438	926	8/5/99

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Article "Outlook on New Transistor Materials," by L. Peters in Semiconductor International, Oct. 1, 2001 edition.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.